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Hashimoto et al.

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(54) **PARALLEL RUNNING CONTROL APPARATUS FOR INVERTER GENERATORS**

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(51) **Int. Cl.**

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H02P 9/04	(2006.01)
H02J 3/40	(2006.01)
H02P 25/22	(2006.01)
H02P 9/02	(2006.01)
H02P 9/00	(2006.01)

(52) **U.S. Cl.**

CPC . ***H02J 3/40*** (2013.01); ***H02P 25/22*** (2013.01); ***H02P 9/02*** (2013.01)

(58) **Field of Classification Search**

USPC .... 290/40 B; 318/400; 322/94; 363/37

See application file for complete search history.

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Primary Examiner — Pedro J Cuevas

(74) *Attorney, Agent, or Firm* — Rankin, Hill & Clark LLP

(57) **ABSTRACT**

In a parallel running control apparatus for inverter generator A having first, second and third inverters adapted convert alternating current outputted from windings wound around an alternator into direct/alternating current by driving switching elements, and CPUs to control turning ON/OFF of the switching elements, it is configured so that the generator A runs in parallel with at least one inverter generator B, which is configured to be same as the inverter generator A, to output a three-phase alternating current, and one of the CPU determines that the generator B was stopped when at least one of phase differences between a phase of an output from the first inverter and phases of outputs from the second and third inverters becomes greater than or equal to a predetermined value.

10 Claims, 14 Drawing Sheets

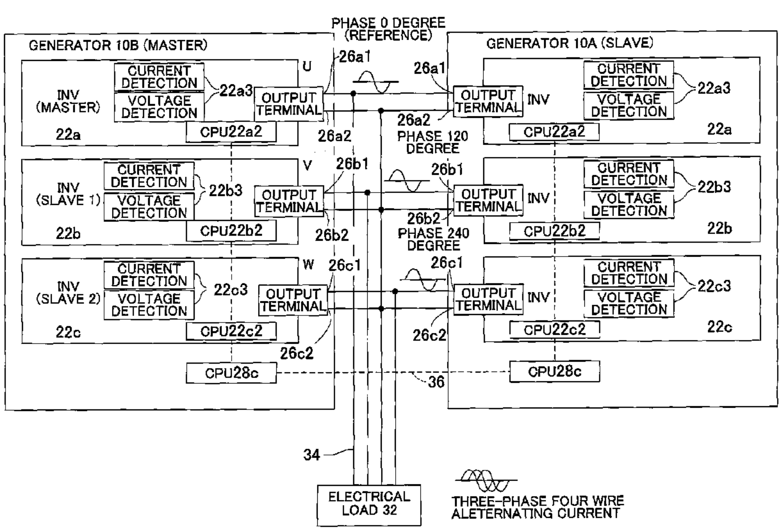


FIG.1

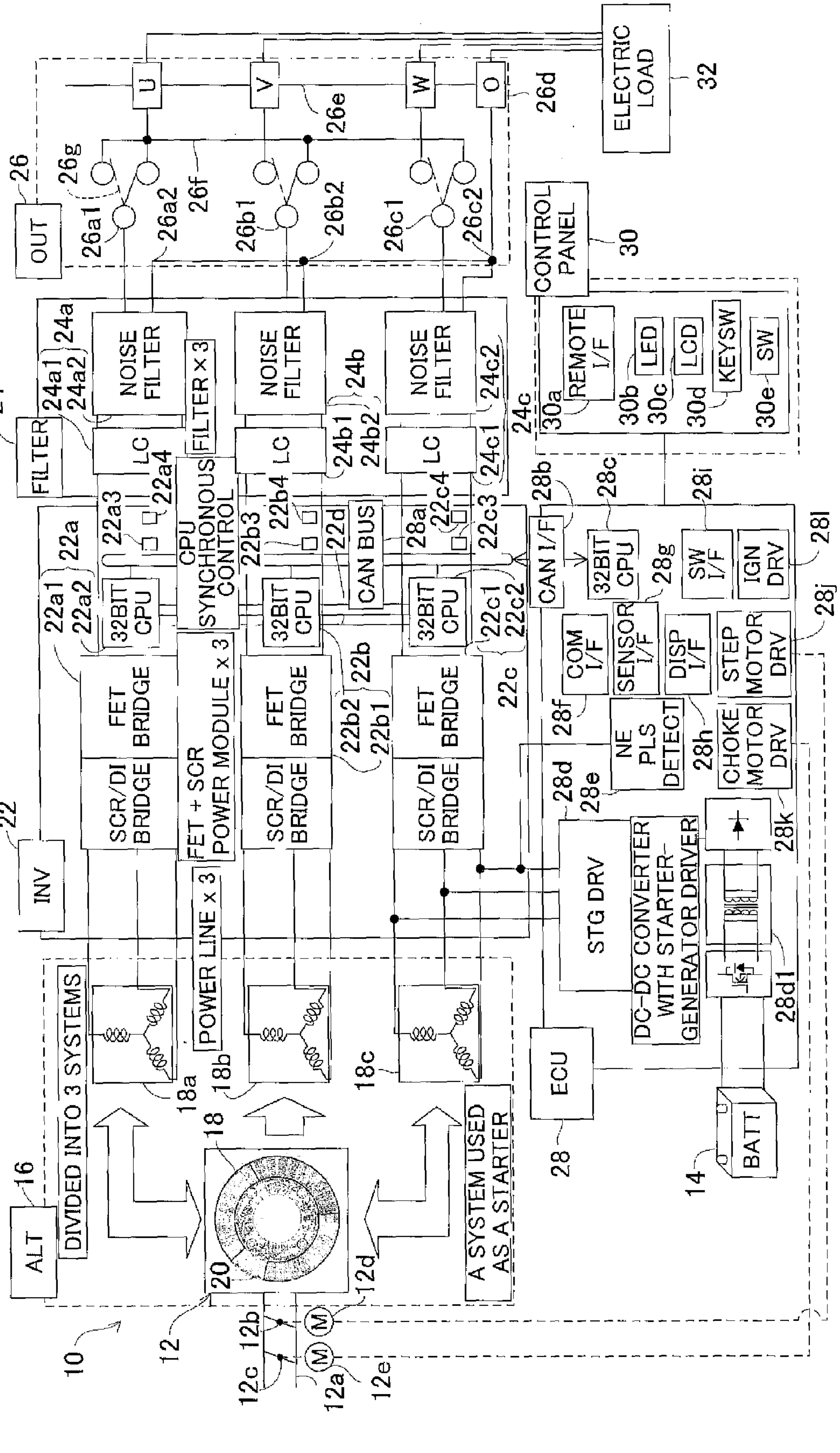

ALT
16
DIVIDED INTO 3 SYSTEMS
A SYSTEM USED AS A STARTER
18
20
12d
12b
12c
12a
12e
12
10
M
18a
18b
18c
POWER LINE × 3
INV
22
SCR/DI BRIDGE
FET BRIDGE
FET + SCR POWER MODULE × 3
32BIT CPU
CPU SYNCHRONOUS CONTROL
CAN BUS
22a
22a1
22a2
22a3
22a4
22b
22b1
22b2
22b3
22b4
22c
22c1
22c2
22c3
22c4
22d
28a
FILTER
24
LC
NOISE FILTER
FILTER × 3
24a
24a1
24a2
24b
24b1
24b2
24c
24c1
24c2
OUT
26
26a1
26a2
26b1
26b2
26c1
26c2
26d
26e
26f
26g
U
V
W
O
ELECTRIC LOAD
32
CONTROL PANEL
30
REMOTE I/F
LED
LCD
KEYSW
SW
30a
30b
30c
30d
30e
CAN I/F
32BIT CPU
SW I/F
IGN DRV
COM I/F
SENSOR I/F
DISP I/F
STEP MOTOR DRV
NE PLS DETECT
CHOKE MOTOR DRV
STG DRV
DC-DC CONVERTER WITH STARTER-GENERATOR DRIVER
28b
28c
28d
28d1
28e
28f
28g
28h
28i
28j
28k
28l
ECU
28
BATT
14

FIG.2

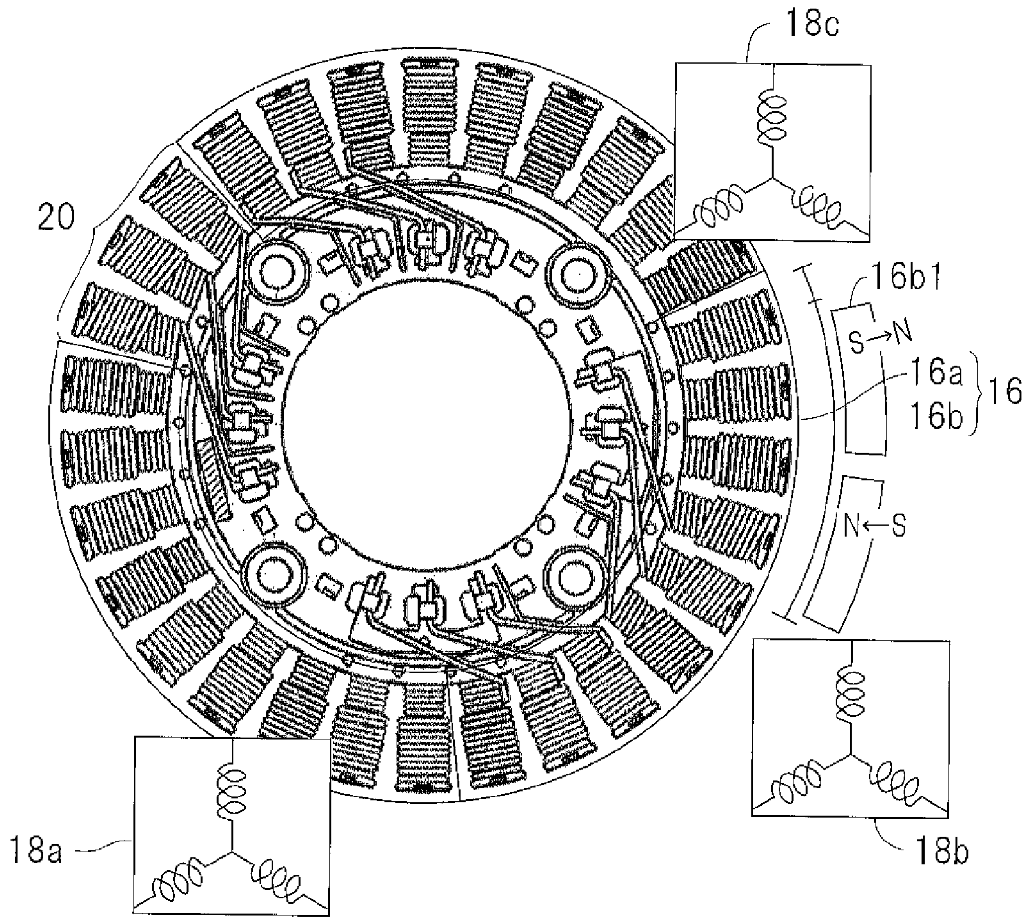


FIG.3

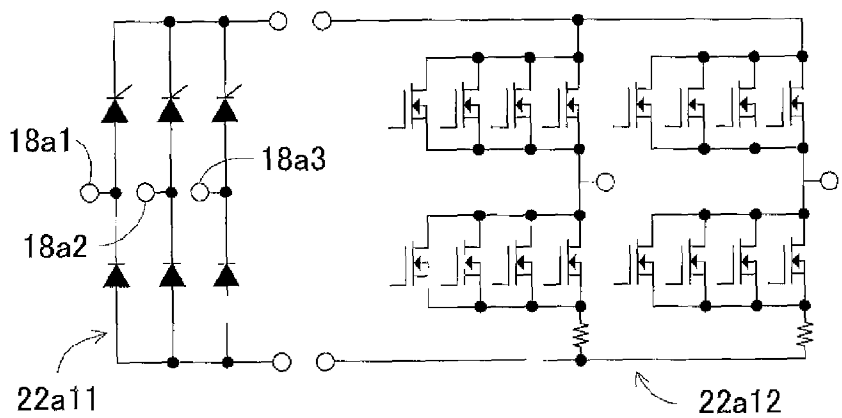

18a1
18a3
18a2
22a11
22a12

FIG.4

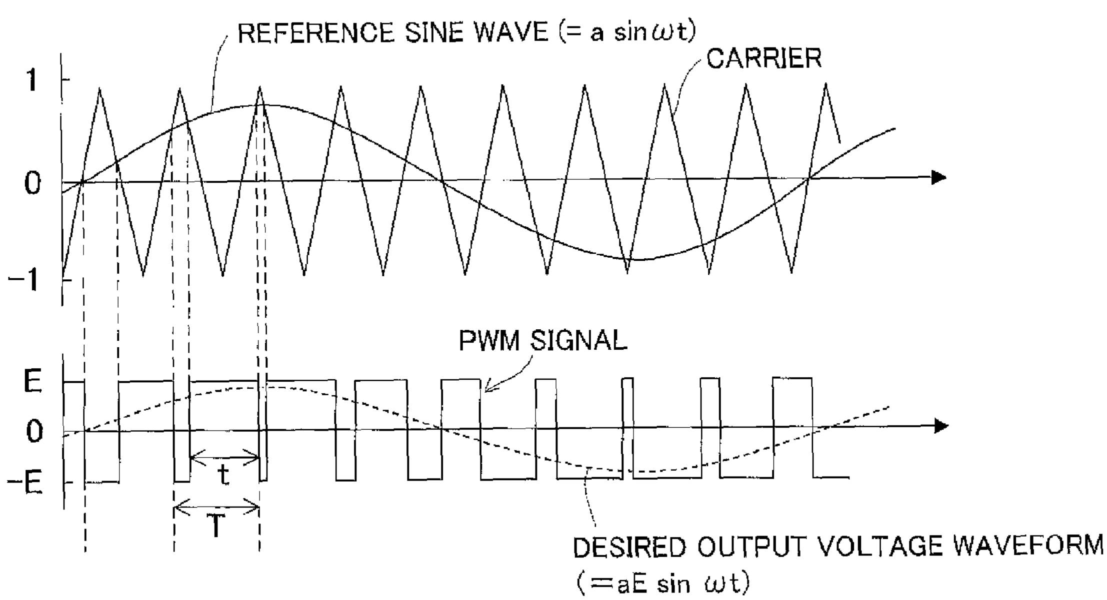

REFERENCE SINE WAVE (= a sinωt)
CARRIER
1
0
-1
PWM SIGNAL
E
0
-E
t
T
DESIRED OUTPUT VOLTAGE WAVEFORM
(=aE sin ωt)

FIG.5

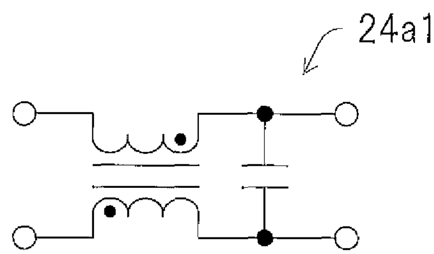


FIG.6

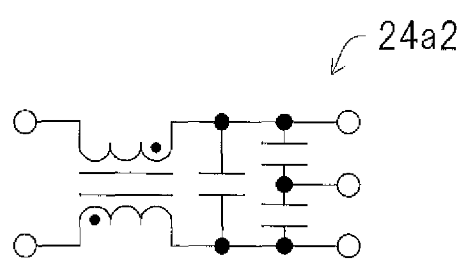


FIG. 7

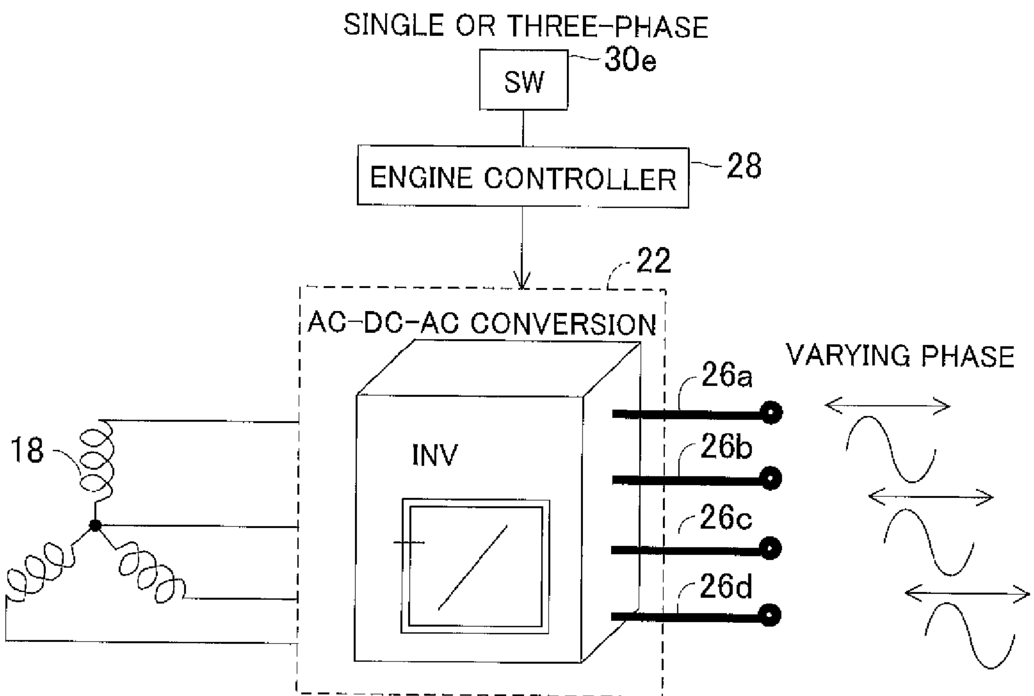

SINGLE OR THREE-PHASE
SW
30e
ENGINE CONTROLLER
28
22
AC-DC-AC CONVERSION
INV
18
26a
26b
26c
26d
VARYING PHASE

FIG. 8

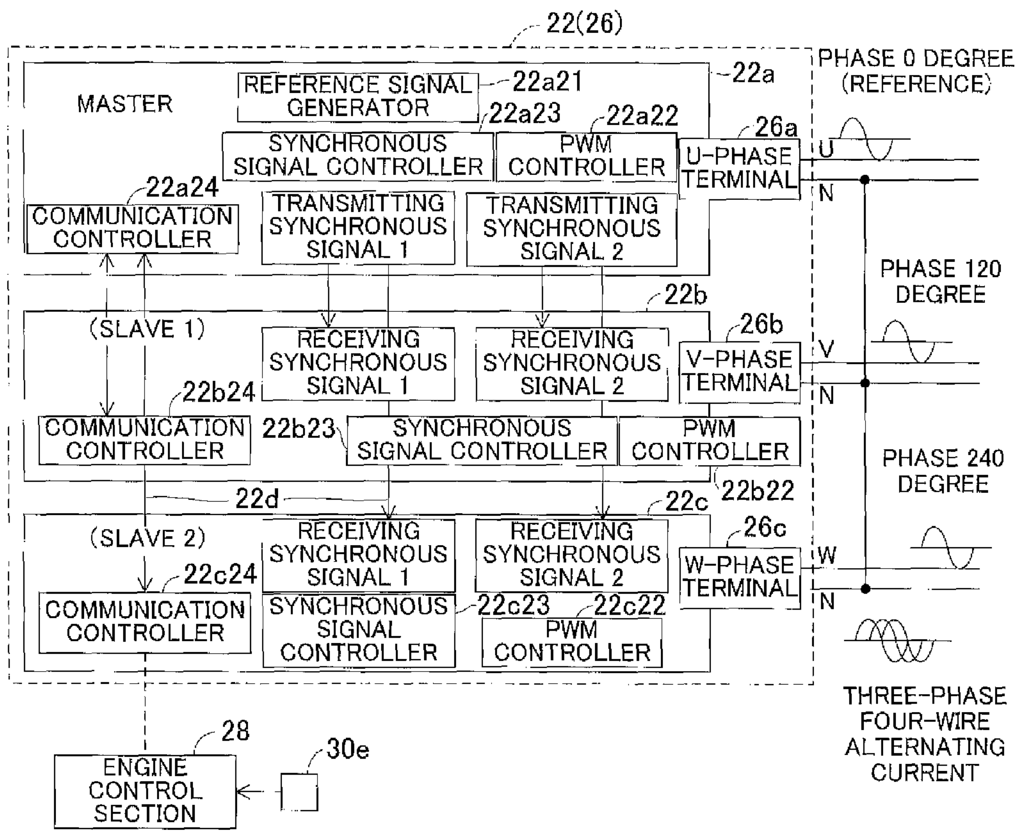

22(26)
MASTER
REFERENCE SIGNAL GENERATOR
22a21
22a
22a23
22a22
SYNCHRONOUS SIGNAL CONTROLLER
PWM CONTROLLER
26a
U-PHASE TERMINAL
PHASE 0 DEGREE (REFERENCE)
U
N
22a24
COMMUNICATION CONTROLLER
TRANSMITTING SYNCHRONOUS SIGNAL 1
TRANSMITTING SYNCHRONOUS SIGNAL 2
22b
PHASE 120 DEGREE
(SLAVE 1)
RECEIVING SYNCHRONOUS SIGNAL 1
RECEIVING SYNCHRONOUS SIGNAL 2
26b
V-PHASE TERMINAL
V
N
22b24
COMMUNICATION CONTROLLER
22b23
SYNCHRONOUS SIGNAL CONTROLLER
PWM CONTROLLER
22b22
PHASE 240 DEGREE
22d
22c
(SLAVE 2)
RECEIVING SYNCHRONOUS SIGNAL 1
RECEIVING SYNCHRONOUS SIGNAL 2
26c
W-PHASE TERMINAL
W
N
22c24
COMMUNICATION CONTROLLER
SYNCHRONOUS SIGNAL CONTROLLER
22c23
22c22
PWM CONTROLLER
THREE-PHASE FOUR-WIRE ALTERNATING CURRENT
28
ENGINE CONTROL SECTION
30e

FIG.9A

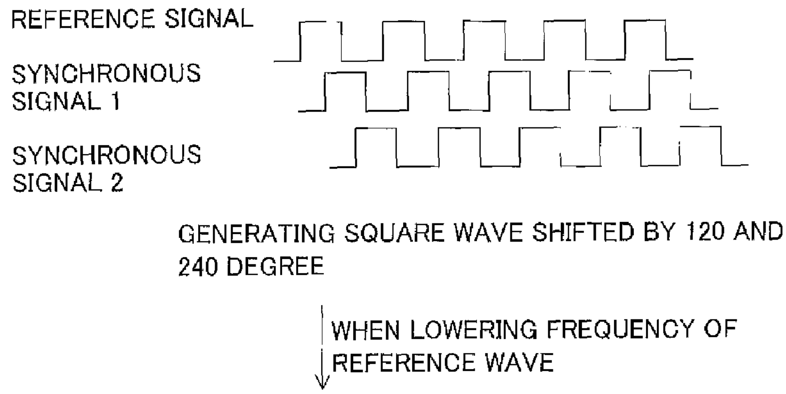

REFERENCE SIGNAL
SYNCHRONOUS SIGNAL 1
SYNCHRONOUS SIGNAL 2
GENERATING SQUARE WAVE SHIFTED BY 120 AND 240 DEGREE
WHEN LOWERING FREQUENCY OF REFERENCE WAVE

FIG.9B

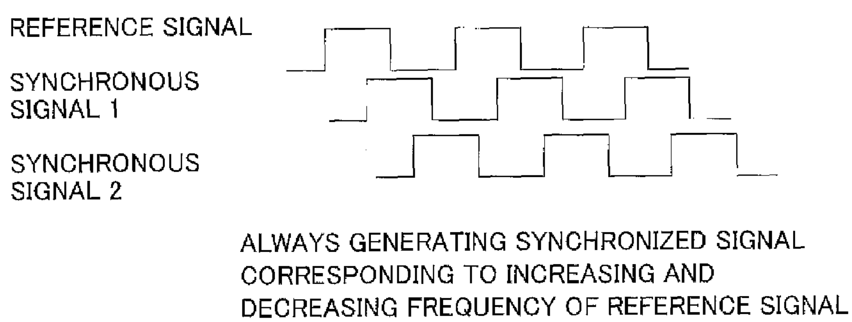

REFERENCE SIGNAL
SYNCHRONOUS SIGNAL 1
SYNCHRONOUS SIGNAL 2
ALWAYS GENERATING SYNCHRONIZED SIGNAL CORRESPONDING TO INCREASING AND DECREASING FREQUENCY OF REFERENCE SIGNAL

FIG. 10

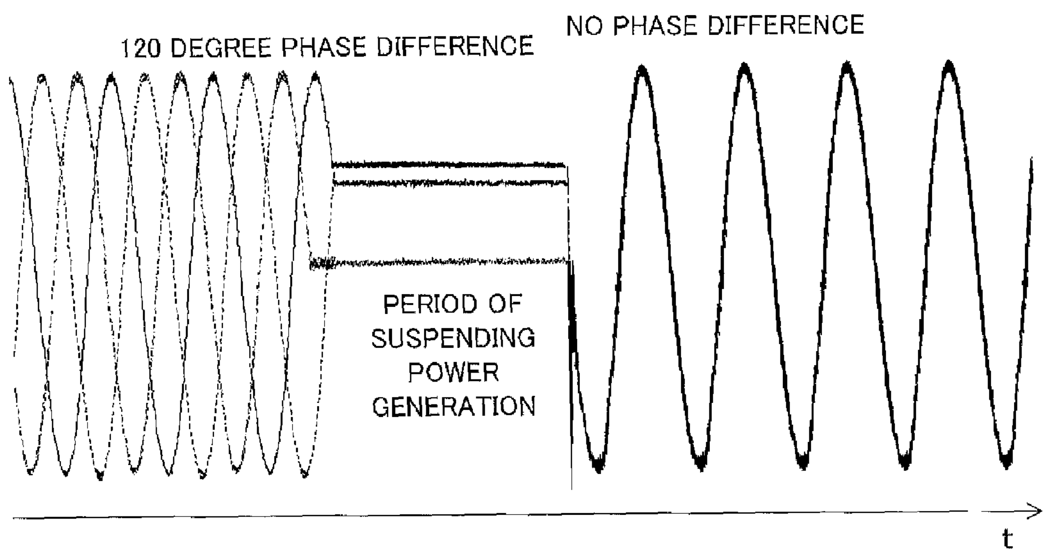

120 DEGREE PHASE DIFFERENCE
NO PHASE DIFFERENCE
PERIOD OF SUSPENDING POWER GENERATION
t

FIG. 11

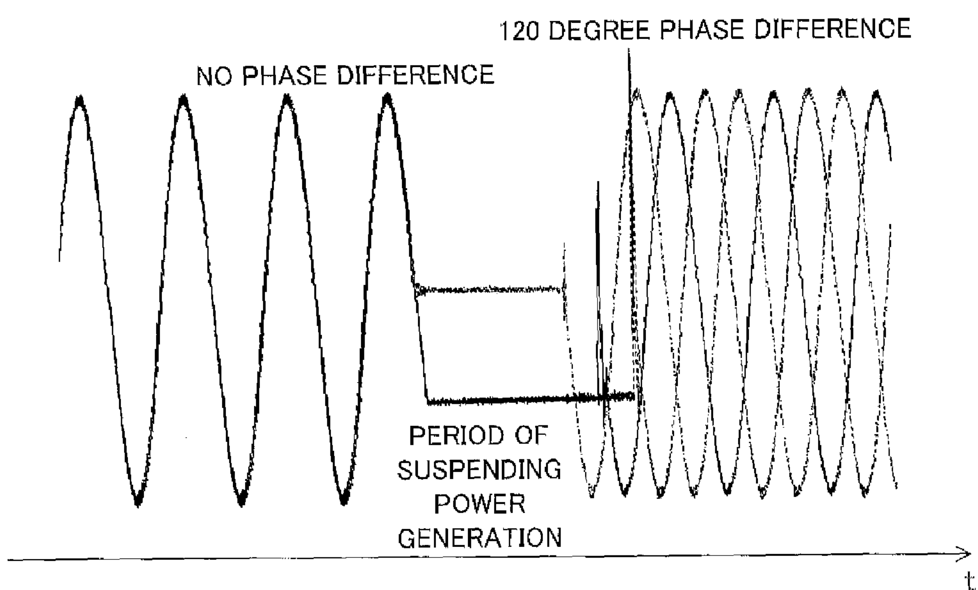

120 DEGREE PHASE DIFFERENCE
NO PHASE DIFFERENCE
PERIOD OF SUSPENDING POWER GENERATION
t

FIG. 12

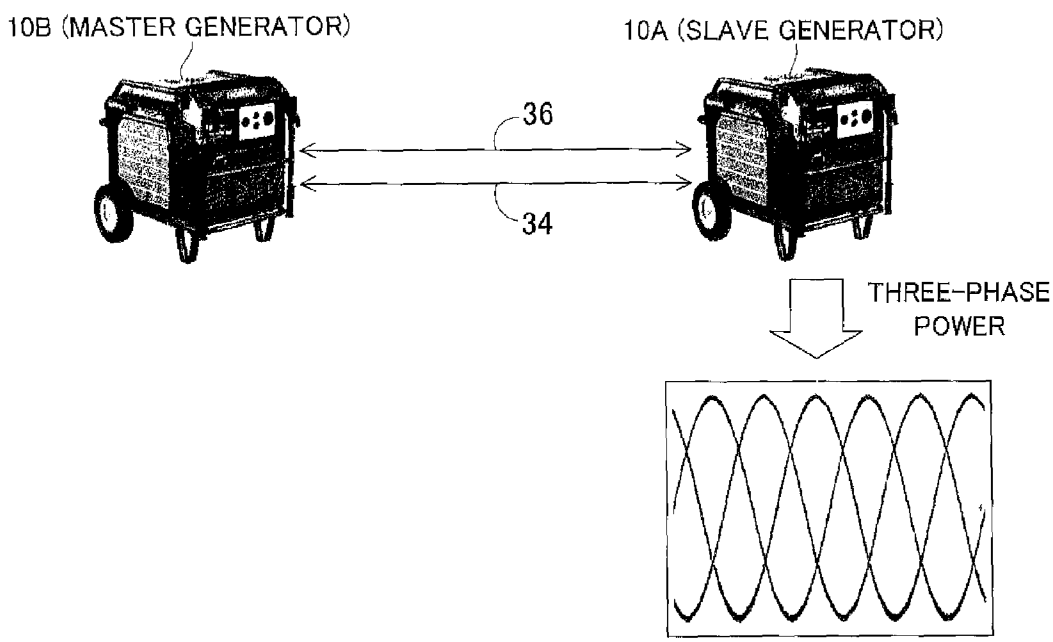

10B (MASTER GENERATOR)
10A (SLAVE GENERATOR)
36
34
THREE-PHASE
POWER

FIG. 13

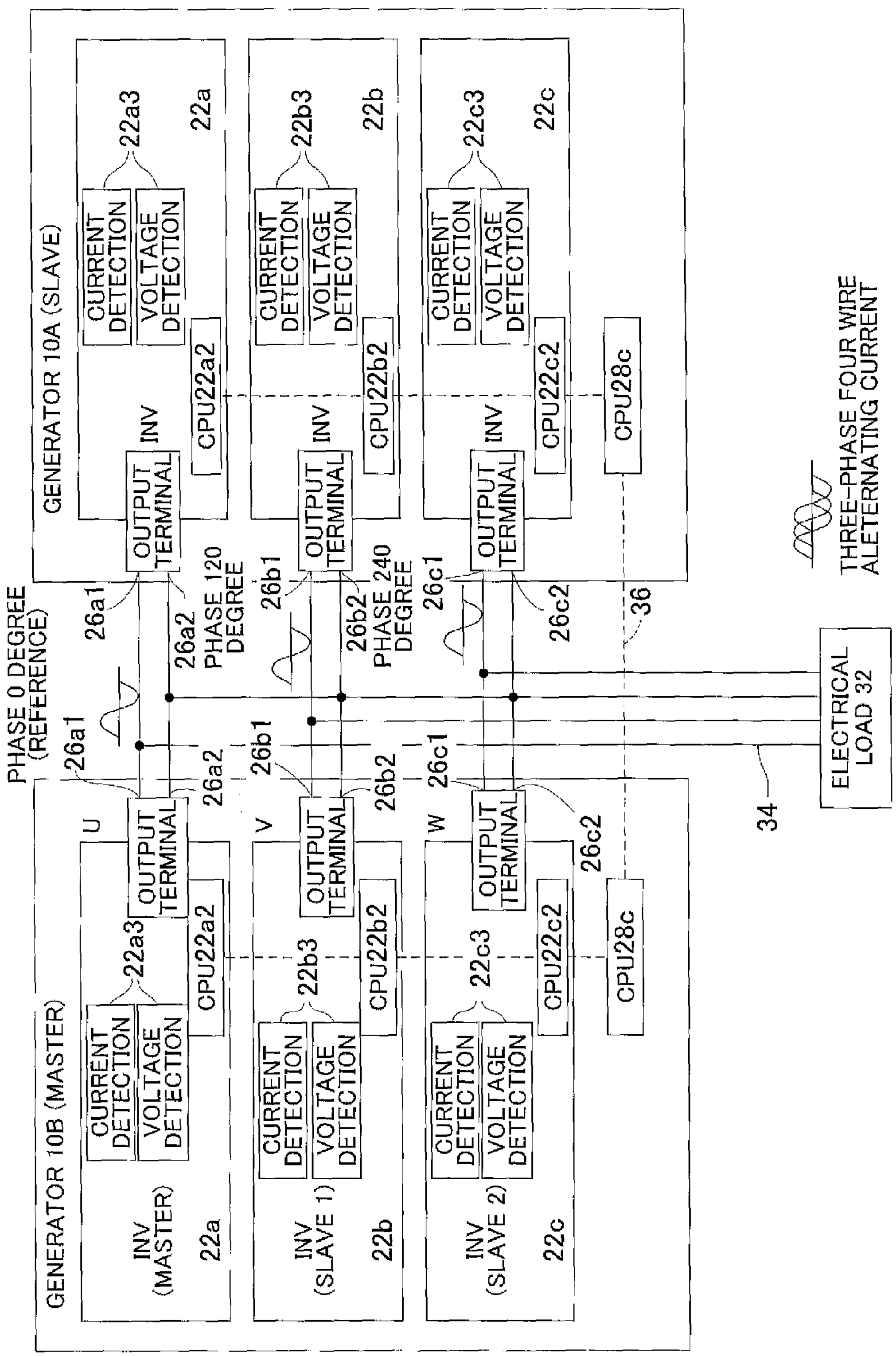

GENERATOR 10A (SLAVE)
CURRENT DETECTION
VOLTAGE DETECTION
22a3
22a
INV
CPU22a2
OUTPUT TERMINAL
22b3
22b
CPU22b2
22c3
22c
CPU22c2
CPU28c
PHASE 0 DEGREE (REFERENCE)
26a1
26a2
PHASE 120 DEGREE
26b1
26b2
PHASE 240 DEGREE
26c1
26c2
36
THREE-PHASE FOUR WIRE ALETERNATING CURRENT
ELECTRICAL LOAD 32
34
GENERATOR 10B (MASTER)
U
V
W
INV (MASTER)
INV (SLAVE 1)
INV (SLAVE 2)

FIG. 14

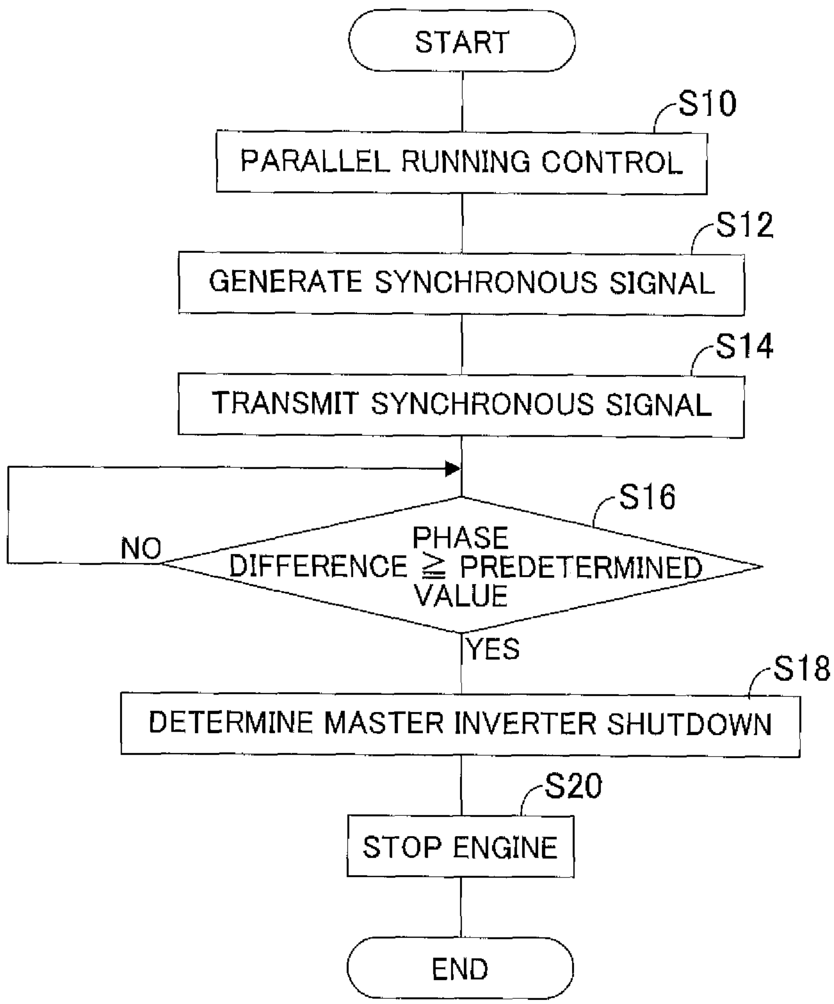

START
S10
PARALLEL RUNNING CONTROL
S12
GENERATE SYNCHRONOUS SIGNAL
S14
TRANSMIT SYNCHRONOUS SIGNAL
S16
PHASE DIFFERENCE ≧ PREDETERMINED VALUE
NO
YES
S18
DETERMINE MASTER INVERTER SHUTDOWN
S20
STOP ENGINE
END

FIG. 15A

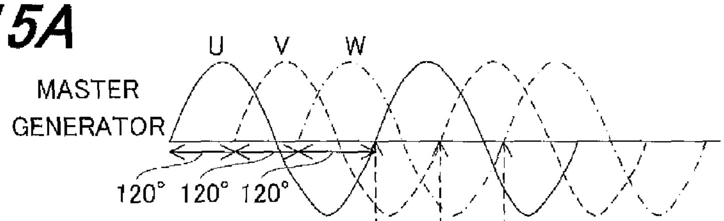


FIG. 15B

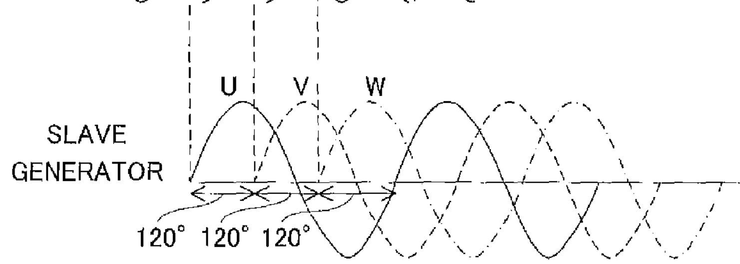


FIG. 16A

FIG. 16B

FIG. 16C

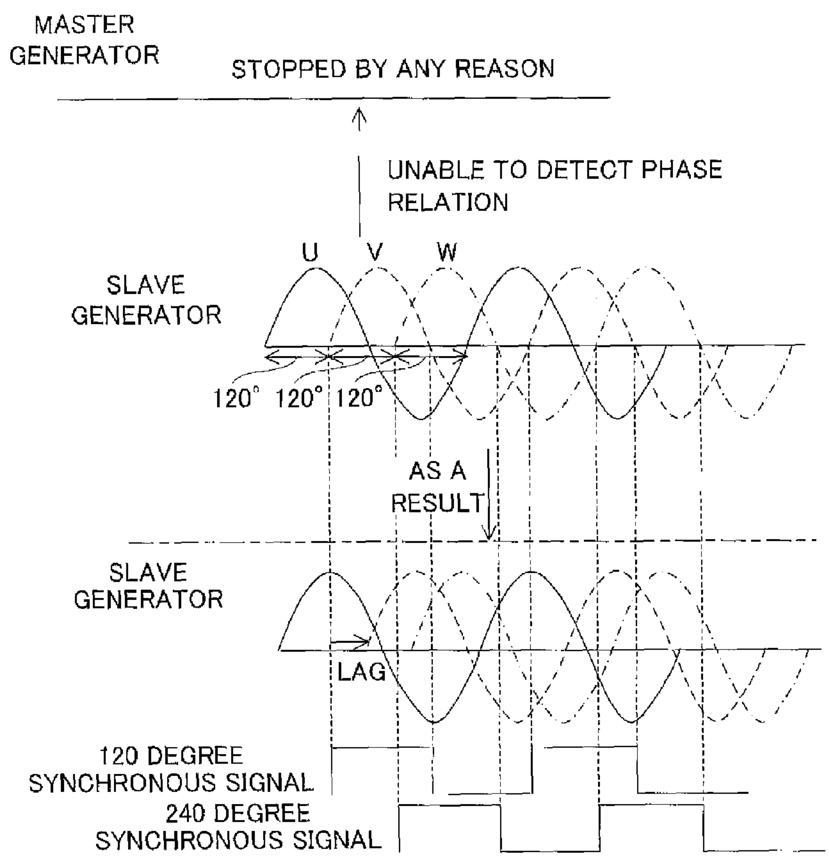


FIG. 17

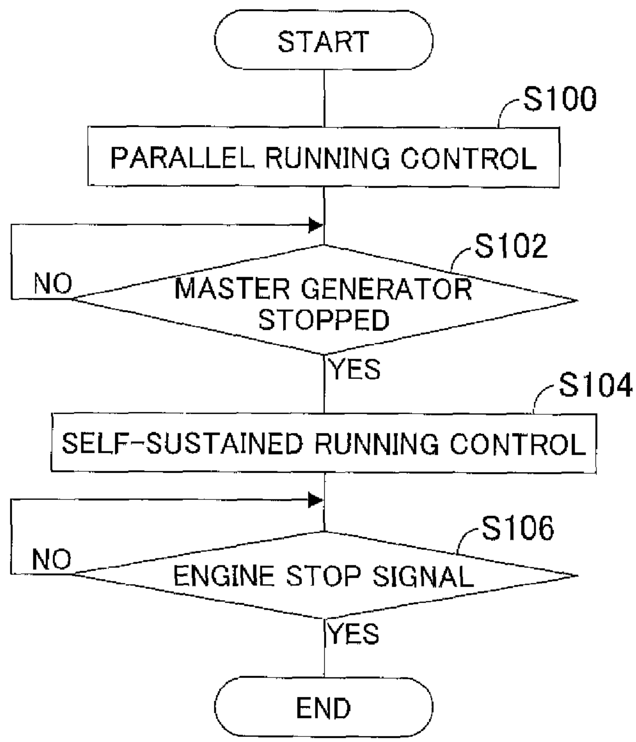
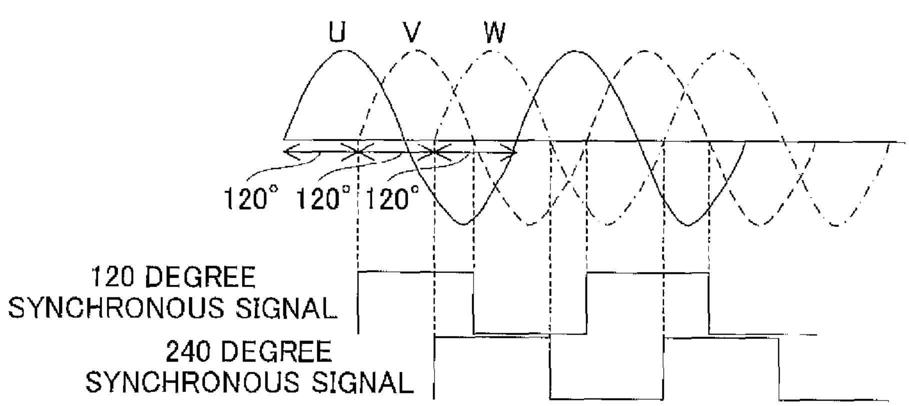

START
S100
PARALLEL RUNNING CONTROL
S102
NO
MASTER GENERATOR STOPPED
YES
S104
SELF-SUSTAINED RUNNING CONTROL
S106
NO
ENGINE STOP SIGNAL
YES
END

FIG. 18


U
V
W
120°
120°
120°
120 DEGREE SYNCHRONOUS SIGNAL
240 DEGREE SYNCHRONOUS SIGNAL

PARALLEL RUNNING CONTROL APPARATUS FOR INVERTER GENERATORS

BACKGROUND OF THE INVENTION

1. Technical Field

Embodiments of the invention relate to a parallel running control apparatus for inverter generators, particularly to a control apparatus that can run inverter generators outputting a three-phase alternating current in parallel

2. Background Art

Conventionally, there is a well-known technique for a parallel running control apparatus for inverter generators, as taught, for example, by Japanese Patent No. 2996542. In the reference, a phase and a voltage amplitude of a single-phase two-wire inverter generator are synchronized with the those of other single-phase two-wire inverter generators, such that the generators are run in parallel.

SUMMARY

Thus the reference discloses running single-phase two-wire inverter generators in parallel by synchronizing their phase and voltage amplitude. However, for three-phase alternating current inverter generators, since it is required to synchronize each phase and each voltage amplitude of a three-phase alternating current of one generator with those of other generator, it is difficult to run three-phase alternating current inverter generators in parallel from the teaching of the reference.

Further, in case of a parallel running control for single-phase two-wire inverter generators, if one of the generators is stopped during the parallel running operation, since the output from the generator is single-phase, it does not cause a phase fluctuation that adversely influences upon a load. However, in a parallel running control apparatus for three-phase inverter generators, since each phase of the power outputs from the generators to be supplied to a load is offset by 120 degrees, if a reference generator is stopped during the parallel running operation, it disadvantageously increases the probability to cause a phase fluctuation of the power output. As a result, a power factor of the load, e.g., a three-phase motor, decreases and the motor becomes unable to generate a normal rotating magnetic field and therefore, unable to operate the load sufficiently. If this happens, the other generator needs to be stopped.

An object of embodiments of this invention is therefore to overcome the foregoing problem by providing a parallel running control apparatus for inverter generators that can run a plurality of three-phase alternating current inverter generators in parallel, while immediately determining whether a reference generator was stopped by any disturbance so as to prevent the load from suffering an adverse influence therefrom.

In order to achieve the object, the embodiments provide in its first aspect a parallel running control apparatus for an inverter generator A having first, second and third windings wound around an alternator driven by an engine, first, second and third inverters each connected to the first, second and third windings to convert alternating current outputted from the first, second and third windings into direct and alternating current through switching elements to output the converted alternating current, first, second and third controllers each adapted to control turning ON/OFF of the switching elements of the corresponding first, second and third inverters and connected to enable to be communicated with each other, and an output terminal connected to terminal groups connected to the first, second and third inverters to output the converted alternating current as one of a U-phase, V-phase, and W-phase outputs and connected to a neutral terminal of the terminal groups; wherein the improvement comprises the inverter generator A is adapted to run in parallel with at least one inverter generator B, which is configured to be same as the inverter generator A, to output a three-phase alternating current, each of the first, second and third controllers has a voltage/phase detector that detects voltage and phase of the converted alternating current inputted into the corresponding first, second and third inverters from the generator B, and when U-phase, V-phase and W-phase terminals of the output terminal are connected to the corresponding U-phase, V-phase and W-phase terminals of the generator B via a connection cable, controls turning ON/OFF of the switching elements of the first, second and third inverters such that the outputs from the first, second and third inverters are synchronized with the detected voltage and phase, and the first controller determines that the generator B was stopped when at least one of phase differences between the converted alternating current output from the first inverter and the converted alternating current output from the second and third inverters becomes greater than or equal to a predetermined value.

In order to achieve the object, the embodiments provide in its second aspect a method for controlling a parallel running operation for inverter generator A having first, second and third windings wound around an alternator driven by an engine, first, second and third inverters each connected to the first, second and third windings to convert alternating current outputted from the first, second and third windings into direct and alternating current through switching elements to output the converted alternating current, first, second and third controllers each adapted to control turning ON/OFF of the switching elements of the corresponding first, second and third inverters and connected to enable to be communicated with each other, an output terminal connected to terminal groups connected to the first, second and third inverters to output the converted alternating current as one of a U-phase, V-phase, and W-phase outputs and connected to a neutral terminal of the terminal groups, and a voltage/phase detector that detects voltage and phase of the converted alternating currents inputted into the first, second and third inverters from a generator B, which is configured to be same as the generator A, and adapted to run in parallel with the generator B, to output a three-phase alternating current; wherein the improvement comprises the steps of controlling turning ON/OFF of the switching elements of the first, second and third inverters such that the outputs from the first, second and third inverters are synchronized with the detected voltage and phase when U-phase, V-phase and W-phase terminals of the output terminal are connected to the corresponding U-phase, V-phase and W-phase terminals of the generator B via a connection cable, and determining that the generator B was stopped when at least one of phase difference between the converted alternating current output from the first inverter and the converted alternating current output from the second and third inverters becomes greater than or equal to a predetermined value.

BRIEF DESCRIPTION OF DRAWINGS

The above and other objects and advantages will be more apparent from the following description and drawings in which:

FIG. **1** is a block diagram showing a parallel running control apparatus for an inverter generator according to a first embodiment of the invention;

FIG. **2** is a plan view showing a crank case of an engine of the inverter generator shown in FIG. **1**;

FIG. **3** is a circuit diagram showing a detailed configuration of an inverter section of the inverter generator shown in FIG. **1**;

FIG. **4** is an explanatory view explaining an operation of the inverter section of the inverter generator shown in FIG. **1**;

FIG. **5** is a circuit diagram showing a detailed configuration of a filter section of the inverter generator shown in FIG. **1**;

FIG. **6** is a circuit diagram similar to FIG. **5**, but showing another detailed configuration of the filter section of the inverter generator shown in FIG. **1**;

FIG. **7** is an explanatory view showing an operation of an engine control section of the inverter generator shown in FIG. **1**;

FIG. **8** is a block diagram specifically showing an operation of a controller of the inverter section of the inverter generator shown in FIG. **1**;

FIGS. **9**A-**9**B are time charts explaining a reference signal and synchronous signals used in the configuration shown in FIG. **8**.

FIG. **10** is a time chart showing waveforms when an output is switched from a three-phase output to a single-phase output in response to the operation shown in FIG. **7**;

FIG. **11** is a time chart showing waveforms when an output is switched from a single-phase output to a three-phase output in response to the operation shown in FIG. **7**;

FIG. **12** is a perspective view of the inverter generators when running two inverter generators shown in FIG. **1** in parallel;

FIG. **13** is a block diagram when connecting the two inverter generators shown in FIG. **12** in parallel;

FIG. **14** is a flowchart showing an operation of a controller during a parallel running operation of the two inverter generators shown in FIG. **12**;

FIGS. **15**A-**15**B are time charts showing output waveforms of generators A and B for explaining processing of the FIG. **14** flowchart during the parallel running operation of the two inverter generators shown in FIG. **12**;

FIGS. **16**A-**16**C are time charts similar to FIGS. **15**A-**15**B, but showing output waveforms of the generators A and B for explaining processing of FIG. **14** during the parallel running operation of the two inverter generators shown in FIG. **12**;

FIG. **17** is a flowchart showing an operation of a controller during a parallel running operation of inverter generators according to a second embodiment of the invention; and

FIG. **18** is a time chart showing output waveforms of generators A and B for explaining processing of the FIG. **17** flowchart.

DESCRIPTION OF EMBODIMENTS

A parallel running control apparatus for inverter generators according to embodiments of the present invention will now be explained with reference to the attached drawings.

FIG. **1** is an overall block diagram showing a parallel running control apparatus for inverter generators according to a first embodiment of the invention.

In FIG. **1**, symbol **10** designates an inverter generator. The generator **10** is equipped with an internal combustion engine **12** and has a rated output of about 5 kW (AC (alternating current) 100V, 50 A). The engine **12** is an air-cooled, spark-ignition gasoline engine.

A throttle valve **12***b* and choke valve **12***c* are installed in an air intake pipe **12***a* of the engine **12**. The throttle valve **12***b* is connected to a throttle motor (composed of a stepper motor) **12***d*, and the choke valve **12***c* is connected to a choke motor (also composed of a stepper motor) **12***e*.

The engine **12** is equipped with a battery **14** whose rated output is about 12V. When power is supplied from the battery **14**, the throttle motor **12***d* and choke motor **12***e* respectively drive the throttle valve **12***b* and choke valve **12***c* to open and close. The engine **12** has an alternator section (shown as "ALT") **16**.

FIG. **2** is a plan view of a crank case **12***f* of the engine **12** shown in FIG. **1**, where the alternator section **16** is provided.

As shown in FIG. **2**, the alternator section **16** includes a stator **16***a* mounted on the crank case **12***f* of the engine **12**, and a rotor **16***b* which is rotatably installed around the stator **16***a* and also functions as a flywheel of the engine **12**.

The stator **16***a* comprises thirty teeth. Twenty-seven teeth of them are wound by three-phase output windings (main windings) **18** comprising of three sets of U, V and W-phase windings, and the other three teeth of them are also wound by one three-phase output winding (sub winding) **20** comprising one set of the U, V, and W-phase windings. The main windings **18** comprise windings **18***a*, **18***b* and **18***c*.

Multiple pairs of permanent magnet pieces **16***b***1** are embedded or attached inside the rotor **16***b* installed on the outer side of the stator **16***a* with radially oriented polarity reversed alternately to face the output windings **18**, **20**. In the alternator section **16**, when the permanent magnet pieces **16***b***1** of the rotor **16***b* are rotated around the stator **16***a*, AC power of the U, V, and W-phase is outputted (generated) from the three-phase output windings **18** (more specifically, **18***a*, **18***b*, **18***c*) and the AC power of each phase is also outputted from the sub winding **20**.

The explanation of FIG. **1** will be resumed. The generator **10** according to this embodiment has, in addition to the alternator section (ALT) **16** where the output windings **18** are wound, an inverter section (shown as "INV") **22**, a filter section (shown as "FILTER") **24**, an output section (shown as "OUT") **26**, an engine control section (shown as "ECU") **28**, and an engine control panel section (shown as "CONTROL PANEL") **30**. The ECU (Electronic Control Unit) functions as an electronic control section and has a CPU as explained later.

As illustrated, the characteristic feature of the generator **10** according to this embodiment is that three sets (three) of single-phase inverter generators (inverters) are connected in parallel so that they can output a three-phase AC of a desired voltage in a desired phase or a single-phase AC of a desired voltage selectively and reliably.

Specifically, the generator **10** has three sets of windings **18** composed of first, second and third windings **18***a*, **18***b*, **18***c*, the inverter section **22** comprising three sets of the inverters composed of first, second and third inverters (inverter generators) **22***a*, **22***b*, **22***c*, the filter section **24** comprising three sets of filters composed of first, second and third filters **24***a*, **24***b*, **24***c*, the output section **26** comprising a three-phase output terminal **26***e* and a single-phase output terminal **26***f*, the engine control section **28** that controls an operation of the engine **12**, and the control panel section **30**.

The inverter section **22** and other sections are provided with, for example, semiconductor chips installed on a printed circuit board accommodated in a case located at an appropriate position of the engine **12**. The control panel section **30** is also provided with semiconductor chips similarly installed at an appropriate position of the engine **12** and a panel connected thereto.

The output windings **18**, the inverter section **22**, the filter section **24** and the output section **26** (each comprising three sets labeled with letters a, b or c) are configured to be connected with the part of the same letter to each other correspondently.

The first, second and third inverters **22***a*, **22***b*, **22***c* constituting the inverter section **22** comprise single-phase two-wire inverters that have power modules **22***a***1**, **22***b***1**, **22***c***1** composed of FETs (Field Effect Transistors) and SCRs (thyristors) integrally connected thereto, 32-bit CPUs **22***a***2** (first controller), **22***b***2** (second controller), **22***c***2** (third controller), and interphase voltage/current sensors **22***a***3**, **22***b***3**, **22***c***3** for detecting voltage and current between phases of a power output. The CPUs **22***a***2**, **22***b***2**, **22***c***2** are connected via a communication path **22***d* with each other to be able to communicate therewith.

FIG. **3** is a circuit diagram showing a configuration of the inverter section **22** in detail. Although the following explanation will be made for the set a, the explanation can also be applied to the sets b and c, since their configurations are basically the same with each other.

As illustrated in FIG. **3**, the power module **22***a***1** comprises a hybrid bridge circuit **22***a***11** in which three SCRs (Thyristors used as switching elements for direct current (DC) conversion) and three DIs (Diodes) are bridge-connected, and an H bridge circuit **22***a***12** in which four FETs are bridge-connected.

Three-phase AC power outputted (generated) from the U-phase winding **18***a* of the output windings **18** wound around the alternator section **16** is inputted to the first inverter **22***a* associated therewith and then inputted to a mid-point between the SCR and DI in the hybrid bridge circuit **22***a***11** of the power module **22***a***1**.

A gate of the SCR in the hybrid bridge circuit **22***a***11** is connected to the battery **14** via a driver circuit (not shown). The CPU **22***a***2** controls current supply (ON; conducted) or termination of the current supply (OFF; not conducted) to the gate of the SCR from the battery **14** through the driver circuit.

Specifically, based on the output of the interphase voltage/current sensor **22***a***3**, the CPU **22***a***2** turns ON (conducts) the gate of the SCR at a turn-on angle (angle of conduction) corresponding to a desired output voltage, such that the AC inputted to the power module **22***a***1** from the output winding **18***a* is converted into DC at the desired output voltage.

The DC outputted from the hybrid bridge circuit **22***a***11** is inputted to the FETs-H bridged circuit **22***a***12** where the FETs are connected to the battery **14**. The CPU **22***a***2** controls current supply (ON; conducted) to the FETs or termination of current supply (OFF; not conducted), the inputted DC is inverted into AC in a desired frequency (e.g., a commercial frequency of 50 Hz or 60 Hz).

FIG. **4** is an explanatory view explaining an operation of the H bridge circuit **22***a***12**.

As illustrated, the CPU **22***a***2** generates a reference sine wave (signal wave; shown by an upper solid-line wave) in a predetermined frequency (i.e., 50 Hz or 60 Hz commercial frequency) of the desired output voltage (in waveform), and compares the generated reference sine wave with a carrier (e.g., a 20 kHz carrier wave) using a comparator (not shown) so as to produce a PWM (Pulse Width Modulation) signal, and turns ON/OFF the FETs in the H bridge circuit **22***a***12** in accordance with the produced PWM signal.

The lower broken-line wave shown in FIG. **4** indicates the desired output voltage (in waveform). It should be noted that the period T (step) of the PWM signal (PWM waveform) is actually much shorter than shown, but is enlarged in FIG. **4** for ease of understanding.

Again returning to the explanation of FIG. **1**, the inverter section **22** is connected to the filter section **24**.

The filter section **24** comprises LC filters (low pass filters) **24***a***1**, **24***b***1**, **24***c***1** that remove a higher harmonic wave and noise filters **24***a***2**, **24***b***2**, **24***c***2** that remove a noise. The AC output inverted in the inverter section **24** is inputted to the LC filters **24***a***1**, **24***b***1**, **24***c***1** and noise filters **24***a***2**, **24***b***2**, **24***c***2** to remove a higher harmonic wave and noise.

FIG. **5** shows a circuit configuration of the LC filter **24***a***1**, and FIG. **6** shows a circuit configuration of the noise filter **24***a***2**. Although not shown, circuit configurations of the LC filters **24***b***1**, **24***c***1** and noise filters **24***b***2**, **24***c***2** are the same.

In FIG. **1**, the inverter section **22** is connected to the output section **26** via the filter section **24**.

As shown in the figure, the output section **26** comprises a three-phase (four-wire) output terminal (output terminal) **26***e* and a single-phase (two-wire) output terminal **26***f*. The three-phase output terminal **26***e* is connected to terminal groups **26***a*, **26***b*, **26***c* which are connected to the first, second and third inverters **22***a*, **22***b*, **22***c* respectively and output one AC in a phase from among U, V, W-phases respectively, and is connected to a neutral terminal **26***d* of the terminal groups in series. The single-phase output terminal (output terminal) **26***f* is connected to the terminal groups in parallel and to the neutral terminal in series.

To be more specific, the three-phase (four-wire) output terminal **26***e* is respectively series-connected to a U-phase terminal **26***a***1** which is connected to the first inverter **22***a* and outputs a U-phase AC, to a V-phase terminal **26***b***1** which is connected to the second inverter **22***b* and outputs a V-phase AC, to a W-phase terminal **26***c***1** which is connected to the third inverter **22***c* and outputs a W-phase AC, and to the neutral O-phase terminal **26***d* which connects neutral points of the first, second and third inverters **22***a*, **22***b*, **22***c*.

Further, the output section **26** has the single-phase (two-wire) output terminal **26***f* which is parallel-connected to the U-phase terminal **26***a***1**, to the V-phase terminal **26***b***1** and to the W-phase terminal **26***c***1**, and is series-connected to the O-phase terminal **26***d*, and has a switching mechanism **26***g* that switches the three-phase output terminal **26***e* and the single-phase output terminal **26***f*.

The three-phase output terminal **26***e* and single-phase output terminal **26***f* are connected to an electric load **32** via a connector (not shown) and the like.

The engine control section **28** has a 32-bit CPU **28***c* and controls operation of the engine **12**. The engine control section **28** is connected to the CPUs **22***a***2**, **22***b***2**, **22***c***2** (first, second and third controllers) of the inverters **22***a*, **22***b*, **22***c* via a CAN (Control Area Network) BUS **28***a* and a CAN I/F (Interface) **28***b* so that it can communicate with the CPUs **22***a***2**, **22***b***2**, **22***c***2**. The output from the aforementioned output winding (sub winding) **20** is supplied to the CPU **22***a***2**, **22***b***2**, **22***c***2**, **28***c* as their operating power.

The engine control section **28** has a starter-generator driver (STG DRV) **28***d* which operates the output winding **18***c*, in addition to the generator, as a starting device (starter) of the engine **12**. Specifically, in this embodiment, one of the output windings **18***a*, **18***b*, **18***c* (e.g., output winding **18***c*) is configured to operate as an engine starter with the aid of the starter-generator driver **28***d*, in other words the alternator section **16** is configured to operate as a prime mover.

The starter-generator driver **28***d* comprises a DC-DC converter **28***d***1**. As described later, the DC-DC converter **28***d***1** boosts the output (raises its voltage) of the battery **14** to about 200V and supplies the boosted battery output to the output winding **18***c* in response to a command from the CPU **28***c* so that the rotor **16***b* of the alternator section **16** is rotated relative to the stator **16***a* to start the engine **12**.

The engine control section **28** further includes a TDC (Top Dead Center) circuit (not shown) to detect pulses outputted from a pulsar (not shown) made of a magnetic pickup installed at location close to the stator **16**a or rotor **16**b, and an engine speed detection circuit **28**e that is connected to a U-phase terminal of the output winding **18**c to detect an engine speed based on the output thereof

The engine control section **28** further includes a communication (COM) I/F **28**f, a sensor (SENSOR) I/F **28**g, a display (DISP) I/F **28**h, a switching (SW) I/F **28**i, a drive circuit **28**j that drives the throttle motor **12**d, a drive circuit **28**k that drives the choke motor **12**e, and an ignition drive circuit **28**l that drives an ignition device (not shown).

The aforementioned 32-bit CPU **28**c determines an opening of the throttle valve **12**b in such a manner that the engine speed converges at a desired engine speed calculated in accordance with required AC output to be supplied to the electric load **32**, and supplies current (power) to the throttle motor **12**d through the drive circuit **28**j to control its operation.

The control panel section **30** has a remote (REMOTE) I/F **30**a which is connected wirelessly (or in wired) to a remote control box **40** provided separately from the engine **12** and adapted to be carried by a user, an LED (Light Emitting Diode) **30**b, an LCD (Liquid Crystal Display) **30**c, a KEY switch (main switch) **30**d which is adapted to be manipulated by the user and to send a command to operate (start) and stop the generator **10**, and a three-phase/single-phase selector switch **30**e which is adapted to send a command to switch the output from the generator **10** between the three-phase AC and single-phase AC.

The control panel section **30** and the engine control section **28** are connected wirelessly (or in wired) to communicate with each other. The outputs of the KEY switch **30**d and selector switch **30**e of the control panel section **30** are inputted to the engine control section **28** through the switching I/F **28**i, and the engine control section **28** controls to flush the LED **30**b and LCD **30**c of the control panel section **30** through the display I/F **28**h.

FIG. **7** is an explanatory view showing an operation of the engine control section **28**.

As described above, since the generator **10** of this embodiment is intended to selectively and reliably output the three-phase AC and single-phase AC at a desired voltage in a desired phase, the inverter section **22** is configured to have three sets of the single-phase inverters (first, second and third inverters) **22**a, **22**b, **22**c, and the CPU **28**c of the engine control section **28** is configured to operate the switching mechanism **26**g of the output section **26** to switch the three-phase output terminal and the single-phase output terminal in response to the output of the selector switch **30**e.

In the inverter section **22**, one of the single-phase inverters **22**a, **22**b, **22**c, e.g., the inverter **22**a, is designated as a master inverter and the others as slave inverters. When the three-phase AC is to be outputted from the generator **10** along with the communication with the CPU **28**c of the engine control section **28**, as shown in FIG. **8**, the CPUs **22**a**2**, **22**b**2**, **22**c**2** of the three sets of the single-phase inverters **22**a, **22**b, **22**c control the operation of the inverter section **22**, making the output phase from the U-phase output terminal **26**a of the master inverter **22**a as a reference, such that the output phases from the V-phase output terminal **26**b and W-phase output terminal **26**c of the slave inverters **22**b, **22**c are offset or delayed from that from the U-phase output terminal **26**a by 120 degrees.

On the other hand, when the single-phase AC is outputted along with the communication with the CPU **28**c, the CPUs **22**a**2**, **22**b**2**, **22**c**2** control the operation of the inverter section **22** to synchronize the outputs from the V-phase output terminal **26**b and W-phase output terminal **26**c of the slave inverters **22**b, **22**c in phase, making the output from the U-phase terminal **26**a of the master inverter **22**a as the reference, such that the single-phase AC is outputted from the single-phase output terminal **26**f.

FIG. **8** is a block diagram showing an operation of the CPUs **22**a**2**, **22**b**2**, **22**c**2**, specifically, an operation of an autonomous running control of the generator, FIGS. **9**A-**9**B are time charts explaining a reference signal and synchronous signals used in the operation of FIG. **8**.

As illustrated, the CPU **22**a**2** of the first (master) inverter **22**a has a reference signal generator **22**a**21** which generates the reference signal (shown in FIGS. **9**A-**9**B) of the predetermined frequency, a PWM controller **22**a**22** which conducts a PWM control in response to the PWM signals described in FIG. **4**, a synchronous signal controller **22**a**23** which generates synchronous signals **1**, **2** (having a predetermined phase difference from the reference signal; shown in FIGS. **9**A-**9**B) that are used to synchronize the output phases of the slave inverters **22**b, **22**c with the output phase of the master inverter **22**a and transmits them to the CPU **22**b**2**, **22**c**2**, and a communication controller **22**a**24** which controls transmitting and receiving (communication of) the generated synchronous signals through the communication path **22**d.

The second and third slave inverters **22**b, **22**c also have, except for the reference signal generator, PWM controllers **22**b**22**, **22**c**22**, synchronous signal controllers **22**b**23**, **22**c**23** and communication controllers **22**b**24**, **22**c**24** which are basically same as those of the master inverter **22**a.

The CPU **22**a**2** of the first (master) inverter **22**a, more specifically its synchronous signal controller **22**a**23** generates the synchronous signals **1**, **2** offset by 120 degrees from the reference signal (in other words, the signals that have predetermined phase differences from the reference signal) and transmits them to the CPUs **22**b**2**, **22**c**2**, if the command to output (switch to) the three-phase AC is sent through the selector switch **30**e. This will be same when the frequency of the reference signal is a predetermined frequency (FIG. **9**A) or lower than the predetermined frequency (FIG. **9**B).

Further, the CPU **22**a**2** of the first (master) inverter **22**a communicates with the CPU **22**b**2**, **22**c**2** and controls the operation of the inverter section **22** to synchronize the V-phase and W-phase outputs from the output terminals **26**b, **26**c with the output phase of the U-phase output terminal **26**a, when the single-phase AC is to be outputted along with the communication with the CPU **28**c, such that the single-phase AC is outputted from the single-phase output terminal **26**f.

Specifically, the CPU **22**a**2** generates the reference signal of the predetermined frequency and the synchronous signals that have a predetermined phase difference (i.e., the same phase) from the reference signal, sends them to the CPUs **22**b**2**, **22**c**2**, and controls the operation of the inverter section **22** to synchronize the V-phase and W-phase outputs from the output terminals **26**b, **26**c with the output phase (reference) of the U-phase output terminal **26**a, such that the single-phase AC is outputted from the single-phase output terminal **26**f.

FIG. **10** is a time chart showing waveforms in a case where the output is switched from the three-phase output to the single-phase output, and FIG. **11** is a time chart showing waveforms in the opposite case. As shown in FIGS. **10** and **11**, the three-phase output and single-phase output of the desired voltage are selectively outputted from the generator **10** in response to the manipulation of the selector switch **30**e of the control panel section **30** by the user.

The characterized aspect of this embodiment of the invention is to provide a parallel running control apparatus for inverter generators that can run a plurality of the aforementioned inverter generators **10** in parallel, which will now be explained.

FIG. **12** is a perspective view of the inverter generators **10** (shown in FIG. **1**), i.e., a plurality of, in specific, two inverter generators **10**A, **10**B to be run in parallel, and FIG. **13** is a block diagram showing an operation of the controllers of the inverter section **22** of the two generators **10**A, **10**B shown in FIG. **12**. In this embodiment, the generator **10**A is designated as a slave generator and the generator **10**B as a master generator.

The generators **10**A, **10**B are connected to each other by a dedicated connection cable **34** and an external communication bus (CANBUS) **36**. It is noted that the CPU **22***a***2** of the first inverter section **22** of the slave generator **10**A functions as a parallel running control apparatus for the generators **10**A, **10**B in this embodiment.

As illustrated in FIG. **13**, the U, V, W-phase terminals **26***a***1**, **26***b***1**, **26***c***1** and their neutral points **26***a***2**, **26***b***2**, **26***c***2** of the generator **10**A are respectively connected to the corresponding U, V, W-phase terminals **26***a***1**, **26***b***1**, **26***c***1** and their neutral points **26***a***2**, **26***b***2**, **26***c***2** of the generator **10**B via the connection cable **34**. The output terminal (three-phase AC output terminal) **26***e* (shown in FIG. **1**) comprises all the terminals of each of the generators **10**A, **10**B and is connected to the electric load **32** via the connection cable **34**.

Specifically, in the generators **10**A, **10**B connected in parallel as illustrated, when the engine **12** of one of the generators, for instance, the slave generator **10**A is started to generate power after the engine **12** of the master generator **10**B is started to generate power, the U, V, W-phase AC each outputted from the inverters **22***a*, **22***b*, **22***c* of the generator **10**B are detected by the corresponding interphase voltage/current sensors **22***a***3**, **22***b***3**, **22***c***3** of the generator **10**A, and the CPUs **22***a***2**, **22***b***2**, **22***c***2** (first, second and third controllers) of the generator **10**A separately control turning ON/OFF of the corresponding switching elements (SCRs in the hybrid bridge circuits **22***a***11**, **22***b***11**, **22***c***11** and FETs in the H bridge circuits **22***a***12**, **22***b***12**, **22***c***12**) based on the detected voltage and current between phases so as to synchronize the each single-phase AC output from the corresponding inverters **22***a*, **22***b*, **22***c* of the generator **10**A with the detected single-phase AC output from the corresponding inverters **22***a*, **22***b*, **22***c* of the generator **10**B in terms of the voltage and phase, thereby running the generators **10**A, **10**B in parallel.

In other words, the CPUs **22***a***2**, **22***b***2**, **22***c***2** of the generator **10**A detect zero-cross timings of the U, V, W-phase AC each outputted from the inverters **22***a*, **22***b*, **22***c* of the generator **10**B based on the output of the interphase voltage/current sensors **22***a***3**, **22***b***3**, **22***c***3** of the generator **10**A, and based on the detected zero-cross timings, separately control turning ON/OFF of the switching elements in the bridge circuits **22***a***12**, **22***b***12**, **22***c***12**, etc., of the first, second and third inverters **22***a*, **22***b*, **22***c*, such that the U, V, W-phase AC each outputted from the corresponding first, second and third inverters **22***a*, **22***b*, **22***c* of own (the generator **10**A) are synchronized with the outputs from the generator **10**B.

Simultaneously, the master generator **10**B operates the abovementioned self-sustained running control. Since the three-phase AC output from the generator **10**B is controlled by the CPU **22***a***2** (first controller) of the generator **10**B, each of the first, second and third controllers **22***a***2**, **22***b***2**, **22***c***2** of the slave generator **10**A only needs to control the output from own first, second and third inverters **22***a*, **22***b*, **22***c* to be synchronized with the outputs from the corresponding each inverter of the generator **10**B in terms of the voltage and phase. With this, the generators **10**A, **10**B can run in parallel with three-phase AC outputs.

The single-phase AC outputs of U, V, W-phases synchronized for each of the corresponding inverters **22** of the generators **10**A, **10**B are supplied to the electric load **32** from the three-phase AC output terminal **26***e* through the connection cable **34**.

As illustrated, since the neutral points **26***a***2**, **26***b***2**, **26***c***2** of the generator **10**A and the corresponding neutral points **26***a***2**, **26***b***2**, **26***c***2** of the generator **10**B are connected to the electric load **32** via the connection cable **34**, the generators **10**A, **10**B run in parallel function as a three-phase four-wire inverter generator and supply the generated power to the electric load **32**.

Further, as illustrated, the generators **10**A, **10**B, more specifically the CPUs **22***a***2**, **22***b***2**, **22***c***2** of the generators **10**A, **10**B are connected with the CANBUS **36** to send and receive data regarding the generated voltage, current, and the like between the master generator **10**B and the slave generator **10**A during the parallel running operation. With this, when the output from one of the master generator **10**B and the slave generator **10**A is lower than the output from the other, the CPUs of the generator with lower output control turning ON/OFF of the FETs in the H bridge circuits **22***a***12**, **22***b***12**, **22***c***12** or the like to correct magnitudes of amplitude and phase offsets of voltage to reduce an unbalanced current, a cross current and the like.

FIG. **14** is a flowchart for explaining the operation of the CPUs **22***a***2**, **22***b***2**, **22***c***2** (first, second and third controllers) of the slave generator **10**A during the parallel running operation of the two inverter generators according to this embodiment. The illustrated program is executed at predetermined intervals, for example 10 milliseconds when the generator **10**A to be run in parallel is started.

The problems to be solved by the embodiments of this invention will be explained again. In the conventional parallel running control apparatus for single-phase two-wire inverter generators, if one of the generators is stopped during the parallel running operation, since the output from the generator is single-phase, it does not cause a phase fluctuation having a negative influence upon a load. However, in a parallel running control apparatus for three-phase inverter generators, since each phase of the power output from the generators to the load is offset by 120 degrees, if a reference generator is stopped during the parallel running operation, it increases the probability to cause a phase fluctuation of the power output, and sometimes makes difficult to supply power to the load sufficiently.

An object of the first embodiment of this invention is therefore to solve the aforementioned problem and to provide a parallel running control apparatus for inverter generators that can run a plurality of three-phase AC inverter generators **10**A in parallel, and while immediately determining whether the master (reference) generator **10**B was stopped by any disturbance to promptly stop the operation of the generators **10**A so as to prevent the load from suffering an adverse influence therefrom.

The program begins at S (Step; Processing step) **10**, in which the abovementioned parallel running control is executed with the master generator **10**B. More specifically, based on the zero-cross timing, voltage, and current of the output from the generator **10**B obtained based on the output of the interphase voltage/current sensors **22***a***3**, **22***b***3**, **22***c***3**, the CPUs **22***a***2**, **22***b***2**, **22***c***2** control turning ON/OFF of the switching elements of the own (subject) first, second and third inverters **22***a*, **22***b*, **22***c* separately to execute the synchronous operation control, so that the single-phase AC outputs from the inverters **22***a*, **22***b*, **22***c* are synchronized with the detected single-phase AC outputs from the corresponding inverters **22***a*, **22***b*, **22***c* of the generator **10**B in terms of the phase and voltage.

FIGS. **15**A-**15**B and FIGS. **16**A-**16**C are time charts showing output waveforms of the generators **10**A, **10**B during the parallel running control. FIG. **15**A shows the output waveforms of the master generator **10**B, and FIG. **15**B shows the output waveforms of the slave generator **10**A to be run in parallel.

As illustrated, when the generator (mater generator) **10**B starts the operation, the CPUs **22***a***2**, **22***b***2**, **22***c***2** of the generator (slave generator) **10**A detect the zero-cross timings of the output phases from the generator **10**B that are inputted into own (their) first, second and third inverters **22***a*, **22***b*, **22***c* through the connection cable **34**, and synchronize the phases of the AC outputs from their first, second and third inverters **22***a*, **22***b*, **22***c* with the phases of the AC outputs from the corresponding first, second and third inverters **22***a*, **22***b*, **22***c* of the generator **10**B, so that the parallel running operation is executed.

The program next proceeds to S**12**, in which the CPU **22***a***2** (first controller) of the generator **10**A makes the AC output from the first inverter **22***a* (U-phase AC) as a reference to generate the synchronous signals so that each of the output phases from the second and third inverters **22***b*, **22***c* are offset by 120 degrees; and to S**14**, in which the generated synchronous signals are transmitted to the CPUs **22***b***2**, **22***c***2** (second and third controllers).

The program next proceeds to S**16**, in which each of the second and third controllers **22***b***2**, **22***c***2** of the generator **10**A detects the zero-cross timings of the AC outputs from the second and third inverters **22***b*, **22***c* and determines whether the phase difference between the detected zero-cross timing and the corresponding synchronous signal transmitted from the first controller **22***a* in S**14** is greater than or equal to the predetermined value. When the result is affirmative, the second or/and the third controller **22***b***2**, **22***c***2** sends a signal to the first controller **22***a***2** to inform that the phase difference between the output phase and the synchronous signal is greater than or equal to the predetermined value.

In S**16**, when the first controller **22***a***2** of the generator **10**A receives the signal from at least one of the second and third controllers **22***b***2**, **22***c***2** informing that the phase difference between the output phase and the corresponding synchronous signal is greater than or equal to the predetermined value, the program proceeds to S**18**, in which it is determined that the master inverter **10**B was stopped (shutdown).

Specifically, as illustrated in FIGS. **16**A-**16**C, in the parallel running control for the inverter generators according to the first embodiment, since the CPU **22***a***2** (first controller) of the slave generator **10**A does not operate the self-sustained running control unlike the CPU **22***a***2** of the master generator **10**B, in a case where the master generator **10**B stops generating power due to any reason, such as a malfunction or the like, the CPUs **22***a***2**, **22***b***2**, **22***c***2** (first, second and third controllers) of the slave generator **10**A become unable to detect the AC output to be made as the reference for synchronization. Hence, as shown in FIG. **16**C, it gradually creates the phase difference (lag) between the AC outputs from the first, second and third inverters **22***a*, **22***b***2**, **22***c***2** of the generator **10**A and the corresponding synchronous signals. Consequently, when the difference (lag) becomes greater than or equal to the predetermined value, it can be determined that the master generator **10**B was stopped.

When it is determined that the master generator **10**B was stopped in S**18**, the program proceeds to S**20**, in which the first controller **22***a***2** of the generator **10**A communicates to the CPU **28***c* of the engine control section **28** to stop the engine **12**, and terminates the illustrated processing.

It should be noted that since the processing in S**16** is repeated until the result becomes affirmative, once the phase difference of the AC output from the generator **10**A becomes greater than or equal to the predetermined value so that it can be determined that the generator **10**B was stopped, in other words, if the generator **10**B is stopped and the phase difference grows to be unable to supply power to the load **32** sufficiently, it can promptly stop the engine **12**.

As mentioned above, in the first embodiment, it is configured to have a parallel running control apparatus for an inverter generator A (**10**A) having first, second and third windings (**18***a*, **18***b*, **18***c*) wound around an alternator (alternator section) **16** driven by an engine (**12**), first, second and third inverters (**22***a*, **22***b*, **22***c*) each connected to the first, second and third windings to convert alternating current outputted from the first, second and third windings into direct and alternating current through switching elements (SCRs in a hybrid bridge circuits **22***a***11**, **22***b***11**, **22***c***11**, FETs in H bridge circuits **22***a***12**, **22***b***12**, **22***c***12**) to output the converted alternating current, first, second and third controllers (CPUs **22***a***2**, **22***b***2**, **22***c***2**) each adapted to control turning ON/OFF of the switching elements of the corresponding first, second and third inverters and connected to enable to be communicated with each other, and an output terminal (**26***e*) connected to terminal groups (**26***a*, **26***b*, **26***c*) connected to the first, second and third inverters to output the converted alternating current as one of a U-phase, V-phase, and W-phase outputs and connected to a neutral terminal of the terminal groups; wherein the improvement comprises: the inverter generator A (**10**A) is adapted to run in parallel with at least one inverter generator B (**10**B), which is configured to be same as the inverter generator A, to output a three-phase alternating current, each of the first, second and third controllers has a voltage/phase detector (**22***a***3**, **22***b***3**, **22***c***3**) that detects voltage and phase of the converted alternating current inputted into the corresponding first, second and third inverters from the generator B, and when U-phase, V-phase and W-phase terminals of the output terminal are connected to the corresponding U-phase, V-phase and W-phase terminals of the generator B via a connection cable (**34**), controls turning ON/OFF of the switching elements of the first, second and third inverters such that the outputs from the first, second and third inverters are synchronized with the detected voltage and phase (S**10**), and the first controller (CPU **22***a***2**) determines that the generator B was stopped when at least one of phase differences between the converted alternating current output from the first inverter and the converted alternating current output from the second and third inverters becomes greater than or equal to a predetermined value (S**12** to S**18**).

With this, without controlling the output phases from the slave generator A to be run in parallel, it becomes possible to run the generators in parallel by synchronizing the AC outputs from own (subject) generator (generator A) with the AC outputs from the generator B in terms of the phase and voltage. As a result, it enables to run the three-phase AC inverter generators in parallel and to immediately determine whether the generator B to be run in parallel was stopped by any disturbance.

Further, the first embodiment is configured so that the first controller (CPU **22***a***2**) generates a synchronous signal having a predetermined phase difference from the converted alternating current output from the first inverter (S**12**) and sends the synchronous signal to the second and third controllers (S**14**), such that the first controller determines that the generator B was stopped when the phase difference between the synchronous signal and the converted alternating current output from at least one of the second and third inverters becomes greater than or equal to the predetermined value (S**16**, S**18**). With this, it becomes possible to accurately determine whether the generator B run in parallel was stopped by any external disturbance.

Further, since the first controller (CPU **22**a**2**) stops the engine (**12**) of the generator A (**10**A) when it is determined that the generator B (**10**B) was stopped, in addition to the above effects, when it is determined that the generator B was stopped during the parallel running operation, it can promptly stop generating power from the own (subject) generator (generator A) to be run in parallel.

Further, since the voltage/phase detector (**22**a**3**, **22**b**3**, **22**c**3**) detects a zero-cross timing of the alternating current inputted into each of the first, second and third inverters from the generator B (**10**B), and the first controller generates the synchronous signal based on the detected zero-cross timing, in addition to the above effects, it becomes possible to reliably operate a phase-synchronous control with the AC outputs from the reference generator B so that the inverter generators can be run in parallel.

The parallel running control apparatus for inverter generators according to a second embodiment of this invention will now be explained.

FIG. **17** is a flowchart explaining an operation of CPUs **22**a**2**, **22**b**2**, **22**c**2** (first, second, third controllers), especially the CPU **22**a**2** of the slave generator **10**A during a parallel running operation of two inverter generators according to the second embodiment of this invention.

In this embodiment, when a phase difference between the AC output from own (subject) second inverter **22**b or own third inverter **22**c and a corresponding synchronous signal becomes greater than or equal to the predetermined value (FIG. **14**, S**18**), the first controller **22**a**2** of the generator **10**A is configured to execute the self-sustained running control by communicating to the second and third controllers **22**b**2**, **22**c**2**.

Similar to the processing from S**10** to S**18** in FIG. **14** of the first embodiment, the program begins at S**100**, in which the parallel running operation with the generator **10**B is started, and proceeds to S**102**, in which it is determined whether at least one of the phase differences (lags) between the zero-cross timings of the AC output from the second and third inverters **22**b, **22**c and the corresponding synchronous signals is greater than or equal to the predetermined value, i.e., determined whether the master generator **10**B was stopped during the parallel running control.

When the result in S**102** is affirmative, the program proceeds to S**104**, in which the parallel running control is terminated and the self-sustained running control is started in accordance with the synchronous signals transmitted to the second and third controllers **22**b**2**, **22**c**2** from the first controller **22**a**2**.

Specifically, the first controller **22**a**2** controls turning ON/OFF of the switching elements to synchronize the zero-cross timings of V-phase and W-phase AC outputted from the own second and third inverters **22**b, **22**c with the generated corresponding synchronous signals to maintain the predetermined phase differences (120 degrees, 240 degrees) from a reference U-phase AC outputted from the first inverter **22**a. In other words, the first controller **22**a**2** of the slave generator **10**A switches the control from the parallel running control to the self-sustained running control which was executed by the first controller **22**a**2** of the master generator **10**B during the parallel running operation.

As described above, after the master generator **10**B was stopped, since there is no reference to be outputted from the master generator **10**B, the first, second and third controllers (CPUs **22**a**2**, **22**b**2**, **22**c) of the slave generator **10**A are unable to maintain a normal parallel running control. However, in the second embodiment of the invention, when it is determined that the master generator **10**B was stopped, it is adapted to terminate the parallel running control and start the self-sustained running control for a single generator. As a result, the power supply to the electric load **32** can be continued by generating power from the own (subject) generator **10**A.

The program next proceeds to S**106**, in which the self-sustained running control is repeatedly continued until a stop signal for the engine **12** is detected.

FIG. **18** is a time chart showing output waveforms of the generators **10**A, **10**B for explaining the processing of the FIG. **17** flowchart, specifically the processing of the self-sustained running control after determining that the master generator **10**B was stopped.

As shown in FIG. **18**, when the master generator **10**B was stopped, the first controller **22**a**2** of the generator **10**A communicates to the second and third controllers **22**b**2**, **22**c**2** to control them and synchronize the zero-cross timings of the V and W-phase AC outputted from the second and third inverters **22**b, **22**c with the corresponding synchronous signals which have 120 degree or 240 degree phase difference from the reference U-phase AC outputted from the first inverter **22**a.

In other aspects, since the configurations and effects are the same as those of the apparatus according to the first embodiment, the explanation thereof will be omitted.

As stated above, the first and second embodiments are configured to have a parallel running control apparatus for an inverter generator A (**10**A) having first, second and third windings (output windings **18**a, **18**b, **18**c) wound around an alternator (alternator section) **16** driven by an engine (**12**), first, second and third inverters (**22**a, **22**b, **22**c) each connected to the first, second and third windings to convert alternating current outputted from the first, second and third windings into direct and alternating current through switching elements (SCRs in a hybrid bridge circuits **22**a**11**, **22**b**11**, **22**c**11**, FETs in H bridge circuits **22**a**12**, **22**b**12**, **22**c**12**) to output the converted alternating current, first, second and third controllers (CPUs **22**a**2**, **22**b**2**, **22**c**2**) each adapted to control turning ON/OFF of the switching elements of the corresponding first, second and third inverters and connected to enable to be communicated with each other, and an output terminal (**26**e) connected to terminal groups (**26**a, **26**b, **26**c) connected to the first, second and third inverters to output the converted alternating current as one of a U-phase, V-phase, and W-phase outputs and connected to a neutral terminal of the terminal groups; wherein the improvement comprises: the inverter generator A (**10**A) is adapted to run in parallel with at least one inverter generator B (**10**B), which is configured to be same as the inverter generator A, to output a three-phase alternating current, each of the first, second and third controllers has a voltage/phase detector (**22**a**3**, **22**b**3**, **22**c**3**) that detects voltage and phase of the converted alternating current inputted into the corresponding first, second and third inverters from the generator B, and when U-phase, V-phase and W-phase terminals of the output terminal are connected to the corresponding U-phase, V-phase and W-phase terminals of the generator B via a connection cable (**34**), controls turning ON/OFF of the switching elements of the first, second and third inverters such that the outputs from the first, second and third inverters are synchronized with the detected voltage and phase (S**10**), and the first controller (CPU **22**a**2**) determines that the generator B was stopped when at least one of phase differences between the converted alternating current output from the first inverter and the converted alternating current output from the second and third inverters becomes greater than or equal to a predetermined value (S**12** to S**18**).

Further, in the embodiments, it is configured so that the first controller (CPU **22**a**2**) generates a synchronous signal having a predetermined phase difference from the converted alternating current output from the first inverter (S**12**) and sends the synchronous signal to the second and third controllers (S**14**), such that the first controller determines that the generator B was stopped when the phase difference between the synchronous signal and the converted alternating current output from at least one of the second and third inverters becomes greater than or equal to the predetermined value (S**16**, S**18**).

Further, in the first embodiment, it is configured so that the first controller (**22**a**2**) stops the engine (**12**) of the generator A (**10**A) when it is determined that the generator B (**10**B) was stopped.

Further, in the second embodiment, it is configured so that the first controller (CPU **22**a**2**) controls the second and third controllers to synchronize the alternating current outputs from the second and third inverters with the synchronous signal when it is determined that the generator B was stopped, such that the operation of the generator A is maintained (S**102** to S**104**).

Further, it is configured so that the voltage/phase detector (**22**a**3**, **22**b**3**, **22**c**3**) detects a zero-cross timing of the alternating current inputted into each of the first, second and third inverters from the generator B (**10**B), and the first controller (CPU **22**a**2**) generates the synchronous signal based on the detected zero-cross timing.

It should be noted that, although the FETs are used as the switching elements of the inverter section **22**, any other switching elements such as IGBTs (Insulated Gate Bipolar Transistors), etc. can be used.

It should also be noted that although the above explanation is made with only focus on the generator **10**A, since the other generator **10**B run in parallel is configured to be the same, even if the generators **10**A and **10**B are swapped, it brings the same effects.

It should also be noted that, in the foregoing embodiments, although a parallel running control apparatus for two generators **10**A, **10**B are explained as an example, the embodiments can be applied for any number of generators.

Japanese Patent Application No. 2011-110571 filed on May 17, 2011, is incorporated by reference herein in its entirety.

While the invention has thus been shown and described with reference to a specific embodiment, it should be noted that the invention is in no way limited to the details of the described arrangements; changes and modifications may be made without departing from the scope of the appended claims.

What is claimed is:

1. A parallel running control apparatus for an inverter generator A having first, second and third windings wound around an alternator driven by an engine, first, second and third inverters each connected to the first, second and third windings to convert alternating current outputted from the first, second and third windings into direct and alternating current through switching elements to output the converted alternating current, first, second and third controllers each adapted to control turning ON/OFF of the switching elements of the corresponding first, second and third inverters and connected to enable to be communicated with each other, and an output terminal connected to terminal groups connected to the first, second and third inverters to output the converted alternating current as one of a U-phase, V-phase, and W-phase outputs and connected to a neutral terminal of the terminal groups;

wherein

the inverter generator A is adapted to run in parallel with at least one inverter generator B, which is configured to be same as the inverter generator A, to output a three-phase alternating current;

each of the first, second and third controllers has a voltage/phase detector that detects voltage and phase of the converted alternating current inputted into the corresponding first, second and third inverters from the generator B, and when U-phase, V-phase and W-phase terminals of the output terminal are connected to the corresponding U-phase, V-phase and W-phase terminals of the generator B via a connection cable, controls turning ON/OFF of the switching elements of the first, second and third inverters such that the outputs from the first, second and third inverters are synchronized with the detected voltage and phase; and

the first controller determines that the generator B was stopped when at least one of phase differences between the converted alternating current output from the first inverter and the converted alternating current output from the second and third inverters becomes greater than or equal to a predetermined value.

2. The apparatus according to claim **1**, wherein the first controller generates a synchronous signal having a predetermined phase difference from the converted alternating current output from the first inverter and sends the synchronous signal to the second and third controllers, such that the first controller determines that the generator B was stopped when the phase difference between the synchronous signal and the converted alternating current output from at least one of the second and third inverters becomes greater than or equal to the predetermined value.

3. The apparatus according to claim **2**, wherein the first controller stops the engine of the generator A when it is determined that the generator B was stopped.

4. The apparatus according to claim **2**, wherein the first controller controls the second and third controllers to synchronize the alternating current outputs from the second and third inverters with the synchronous signal when it is determined that the generator B was stopped, such that the operation of the generator A is maintained.

5. The apparatus according to claim **2**, wherein the voltage/phase detector detects a zero-cross timing of the alternating current inputted into each of the first, second and third inverters from the generator B; and

the first controller generates the synchronous signal based on the detected zero-cross timing.

6. A method for controlling a parallel running operation for inverter generator A having first, second and third windings wound around an alternator driven by an engine, first, second and third inverters each connected to the first, second and third windings to convert alternating current outputted from the first, second and third windings into direct and alternating current through switching elements to output the converted alternating current, first, second and third controllers each adapted to control turning ON/OFF of the switching elements of the corresponding first, second and third inverters and connected to enable to be communicated with each other, an output terminal connected to terminal groups connected to the first, second and third inverters to output the converted alternating current as one of a U-phase, V-phase, and W-phase outputs and connected to a neutral terminal of the terminal groups, and a voltage/phase detector that detects voltage and phase of the converted alternating currents inputted into the first, second and third inverters from a generator B, which is configured to be same as the generator A, and adapted to run in parallel with the generator B, to output a three-phase alternating current,

the method comprising the steps of:

controlling turning ON/OFF of the switching elements of the first, second and third inverters such that the outputs from the first, second and third inverters are synchronized with the detected voltage and phase when U-phase, V-phase and W-phase terminals of the output terminal are connected to the corresponding U-phase, V-phase and W-phase terminals of the generator B via a connection cable; and

determining that the generator B was stopped when at least one of phase difference between the converted alternating current output from the first inverter and the converted alternating current output from the second and third inverters becomes greater than or equal to a predetermined value.

7. The method according to claim **6**, further comprising the steps of:

generating a synchronous signal having a predetermined phase difference from the converted alternating current output from the first inverter; and

sending the synchronous signal to the second and third controllers,

wherein the step of determining determines that the generator B was stopped when the phase difference between the synchronous signal and the converted alternating current output from at least one of the second and third inverters becomes greater than or equal to the predetermined value.

8. The method according to claim **7**, further comprising the step of:

stopping the engine of the generator A when it is determined that the generator B was stopped.

9. The method according to claim **7**, wherein the step of controlling controls the second and third controllers to synchronize the alternating current outputs from the second and third inverters with the synchronous signal when it is determined that the generator B was stopped, such that the operation of the generator A is maintained.

10. The method according to claim **7**, further comprising the step of:

detecting a zero-cross timing of the alternating current inputted into each of the first, second and third inverters from the generator B,

wherein the step of generating generates the synchronous signal based on the detected zero-cross timing.

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